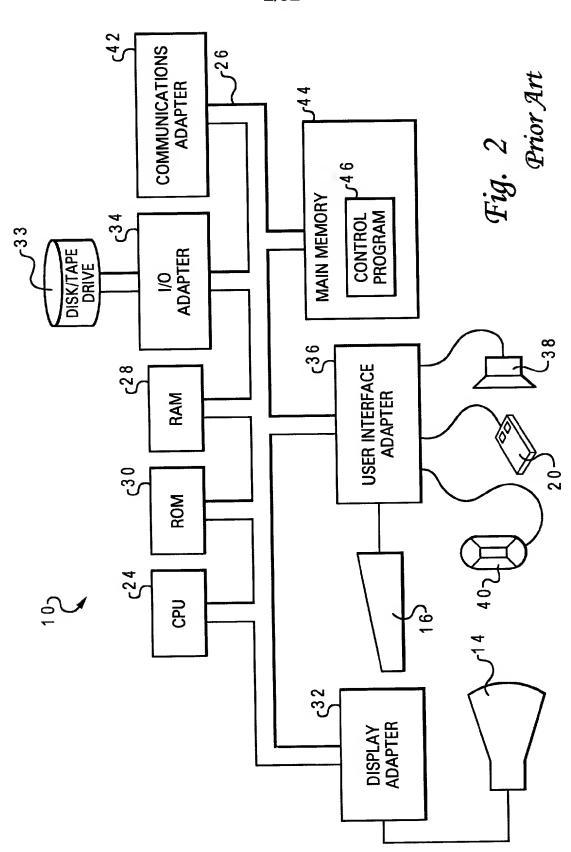


Fig. 1 Prior Art



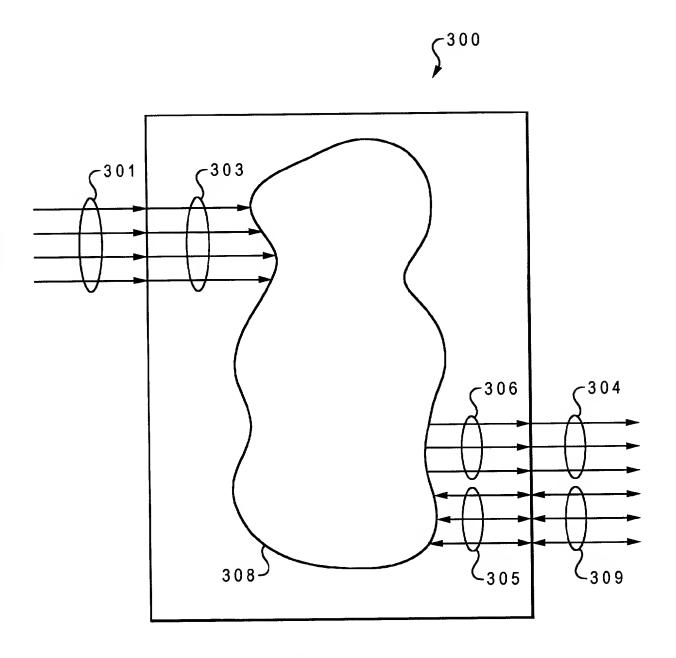
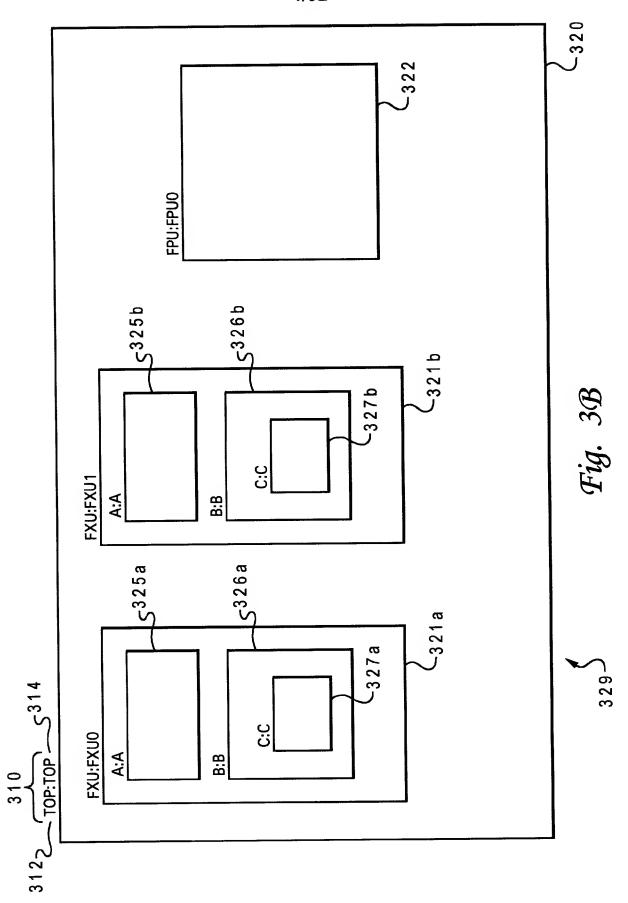
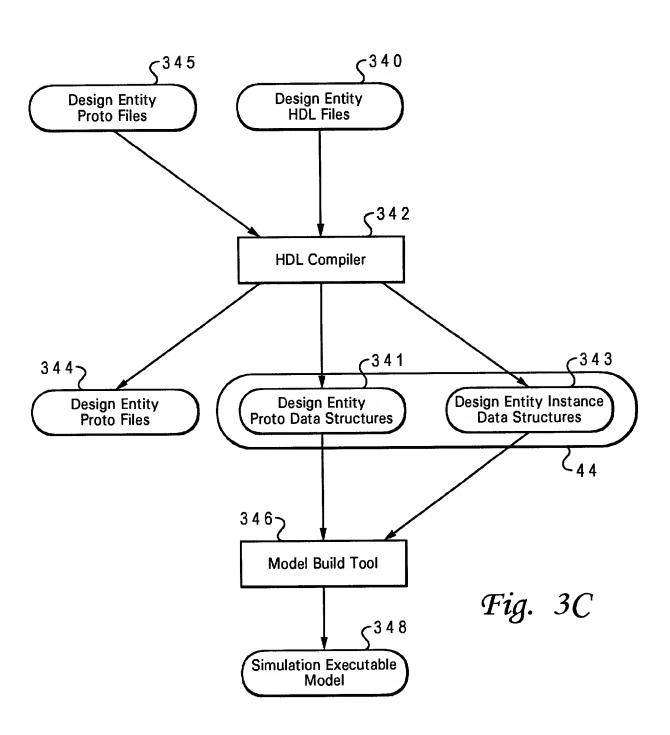


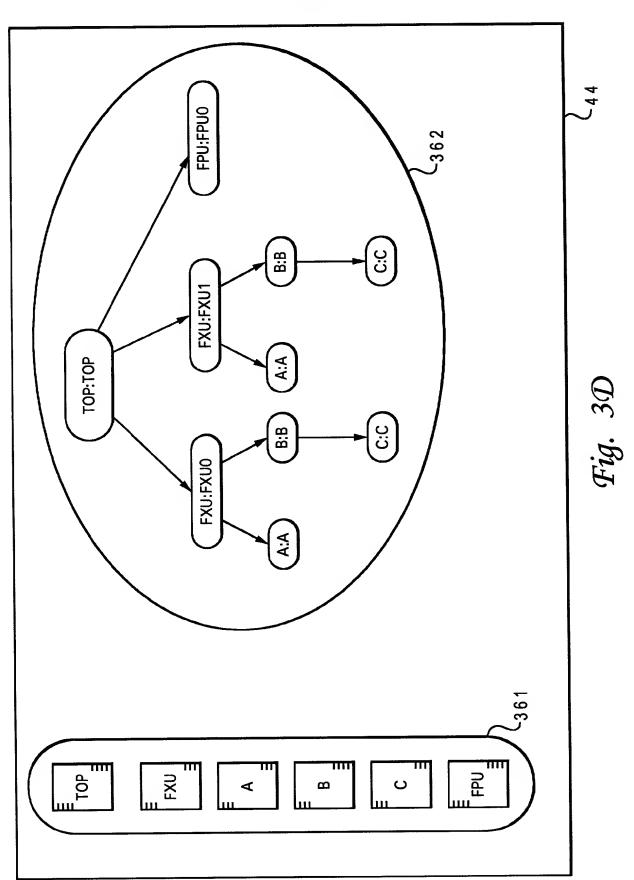
Fig. 3A

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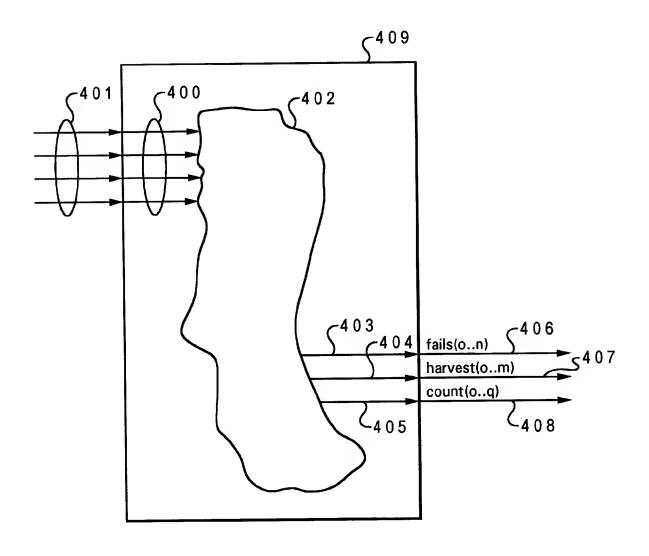
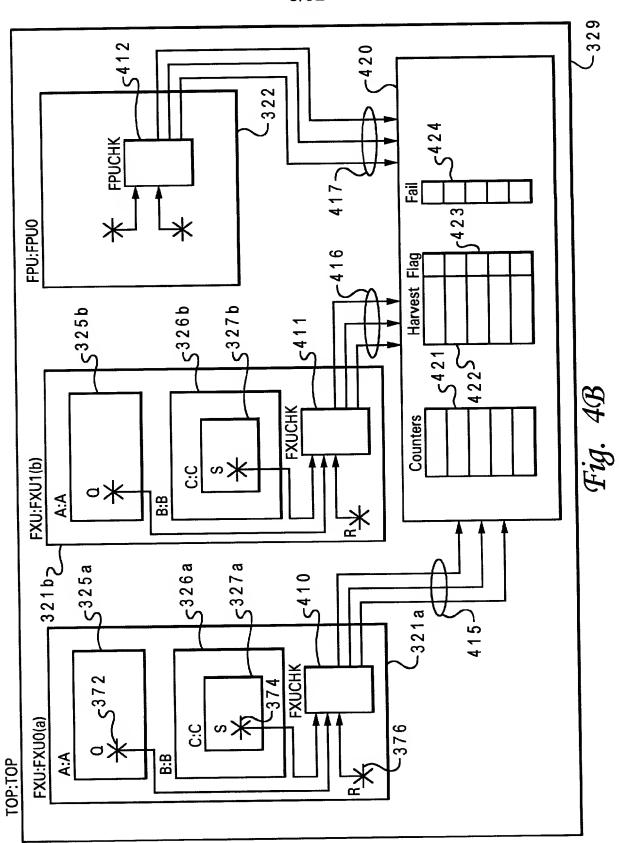


Fig. 4A

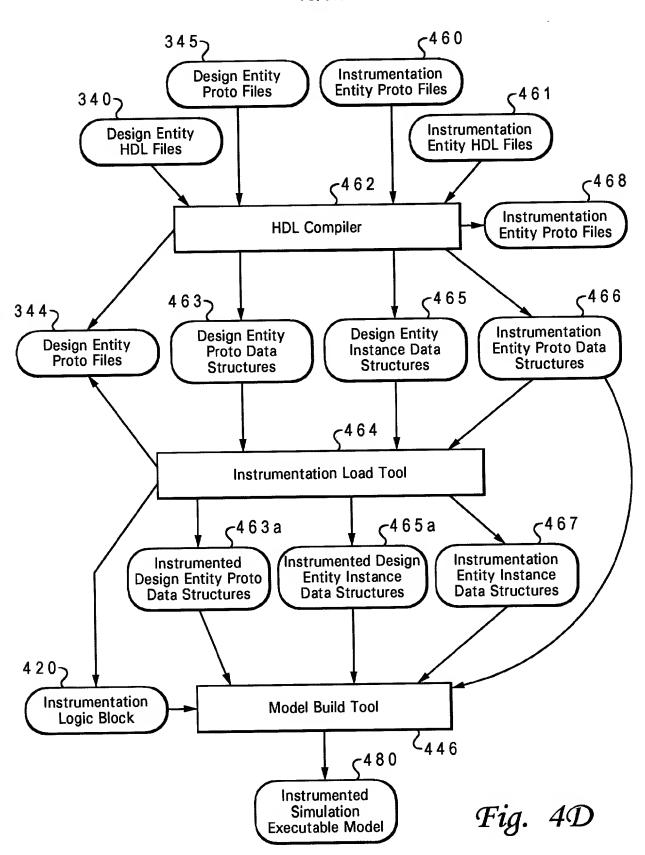


```
ENTITY FXUCHK IS
                  PORT(
                               SIN
                                                      IN std_ulogic;
                               Q IN
                                                      IN std ulogic;
                               R^{-}IN
                                                      IN std ulogic;
                                                                                                    450
                               clock
                                                      IN std ulogic;
                                                      OUT std_ulogic_vector(0 to 1);
                               fails
                                                       OUT std ulogic vector(0 to 2);
                               counts
                               harvests
                                                       OUT std ulogic vector(0 to 1);
                          );
          --!! BEGIN
--!! Design Entity: FXU;
           --!! inputs
           --!! S IN
                                           B.C.S;
          --!! Q_IN =>
--!! R_IN =>
--!! CLOCK =>
--!! End Inputs
                                           A.Q;
                                           clock;
           --!! Fail Outputs;
         --!! 0 : "Fail message for failure event 0";

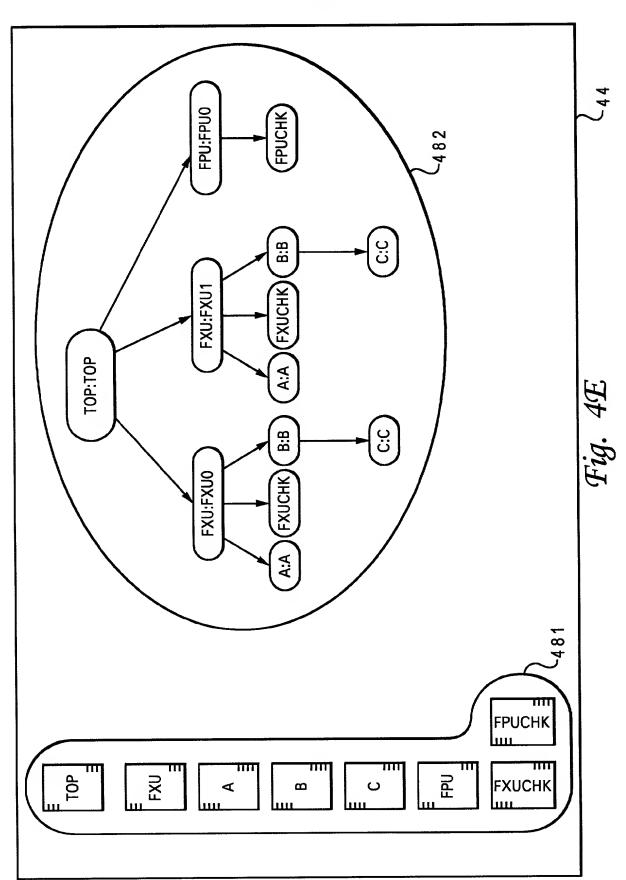
--!! 1 : "Fail message for failure event 1";

--!! End Fail Outputs;
                                                                                                              -440
                                                                         451
           --!! Count Outputs;
          --!! 0 : <event0> clock;
--!! 1 : <event1> clock;
           --!! 2: <event2> clock;
           --!! End Count Outputs;
           --!! Harvest Outputs;
4 5 6 --!! 0 : "Message for harvest event 0";
--!! 1 : "Message for harvest event 1";
--!! End Harvest Outputs;
457 √ --!! End;
           ARCHITECTURE example of FXUCHK IS
           BEGIN
                  ... HDL code for entity body section ...
           END;
```

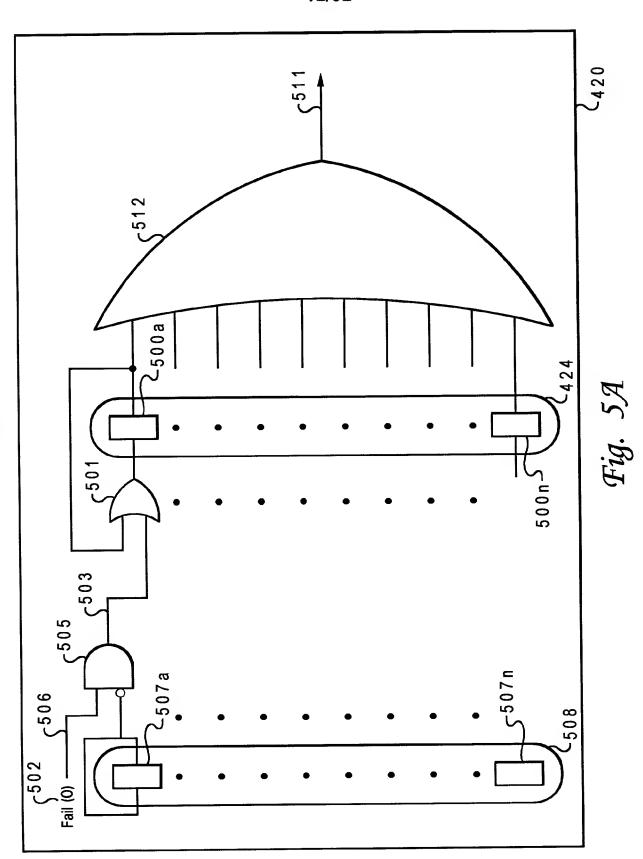
Fig. 40



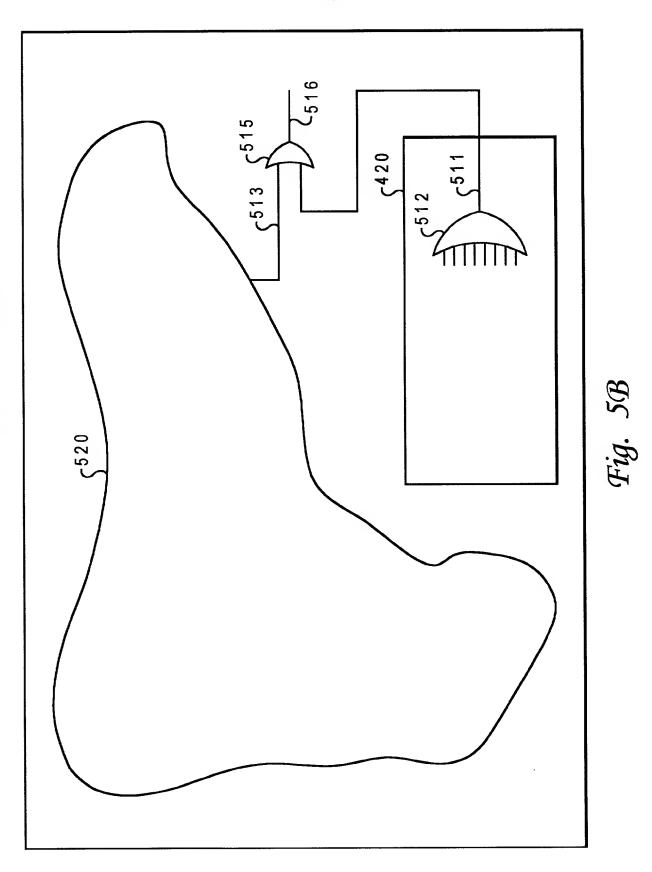
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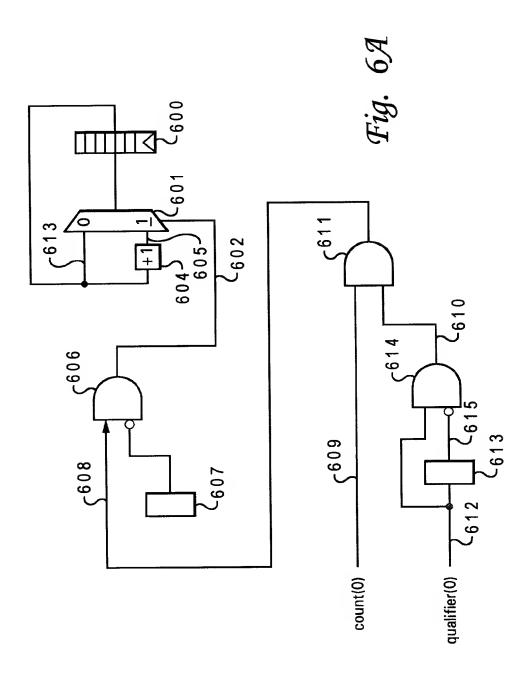
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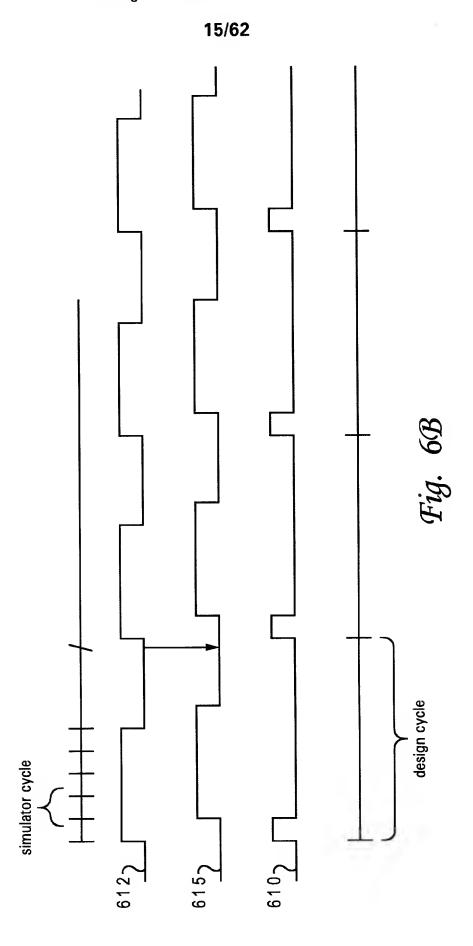


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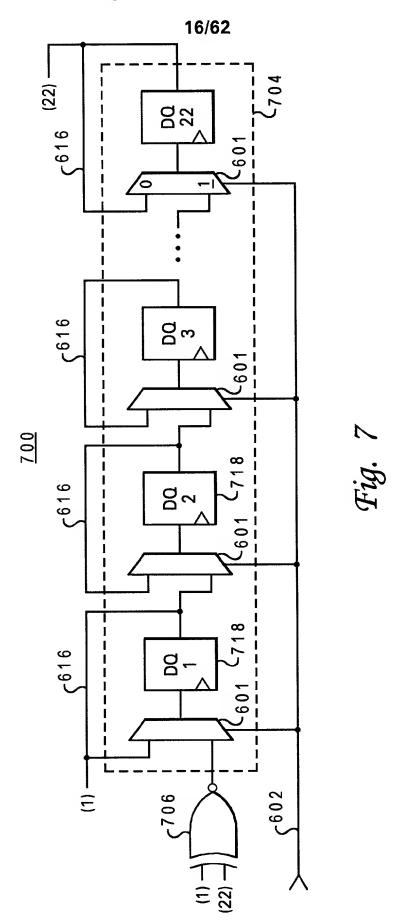


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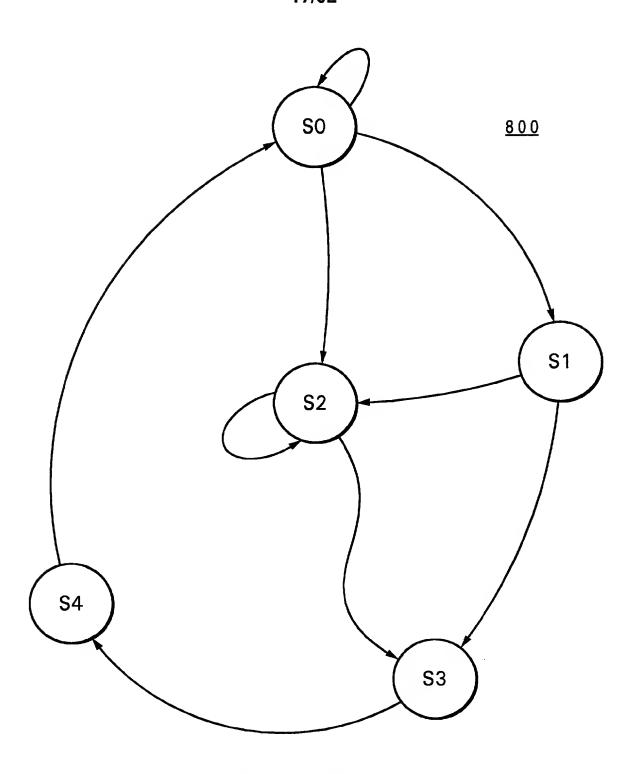


Fig. 8A
Prior Art

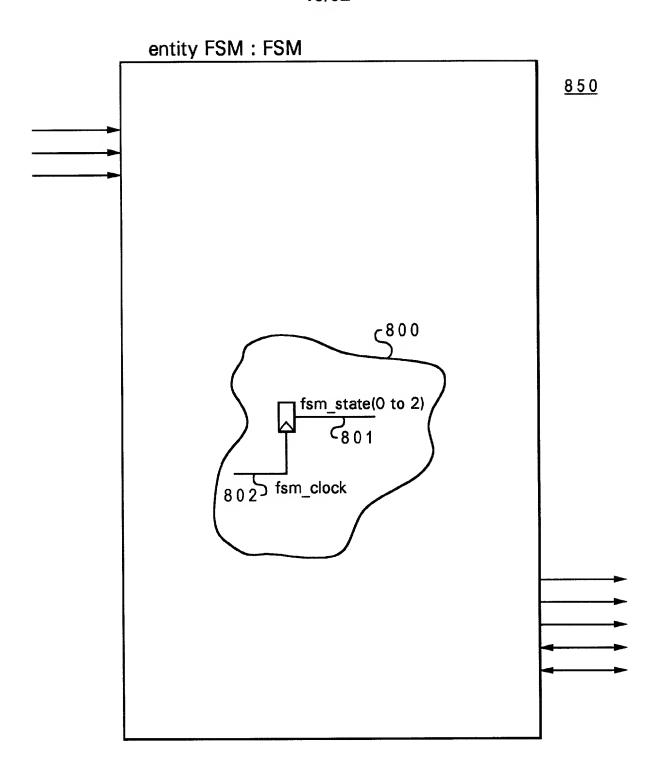


Fig. 8B
Prior Art

```
ENTITY FSM IS
    PORT(
              ....ports for entity fsm....
          );
     ARCHITECTURE FSM OF FSM IS
     BEGIN
              ... HDL code for FSM and rest of the entity ...
              fsm_state(0 to 2) <= ... Signal 801 ...
      853 < --!! Embedded FSM : examplefsm;
                          : (fsm_clock);
      859 \{ --!! clock
      854 \{ --!! state_vector : (fsm_state(0 to 2));
      8 5 5 √ --!! states
                          : (S0, S1, S2, S3, S4);
                                                                       852
      856 \( --!! \) state encoding : ('000', '001', '010', '011', '100');
                            : (S0 = > S0, S0 = > S1, S0 = > S2,
            --!! arcs
                               (S1 = > S2, S1 = > S3, S2 = > S2,
                               (S2 = > S3, S3 = > S4, S4 = > S0);
      858 --!! End FSM;
     END;
```

Fig. 80

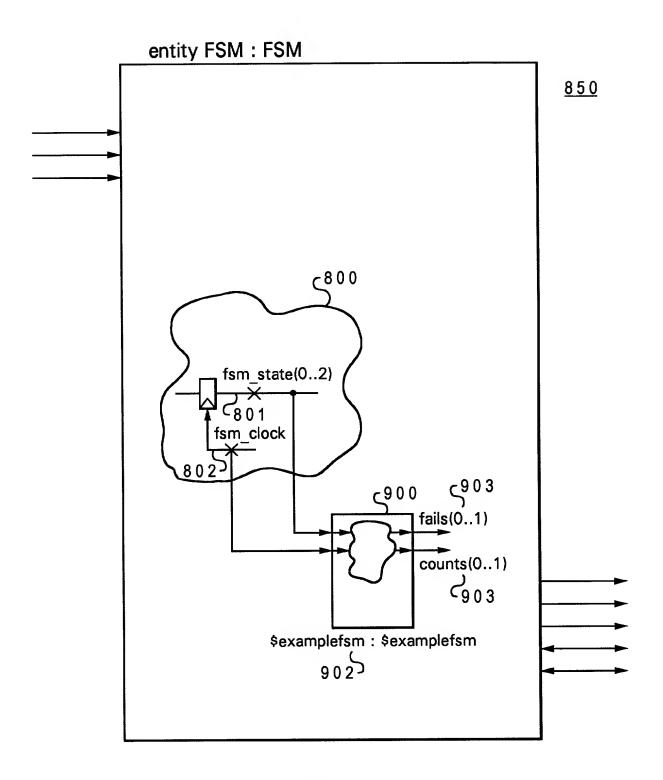
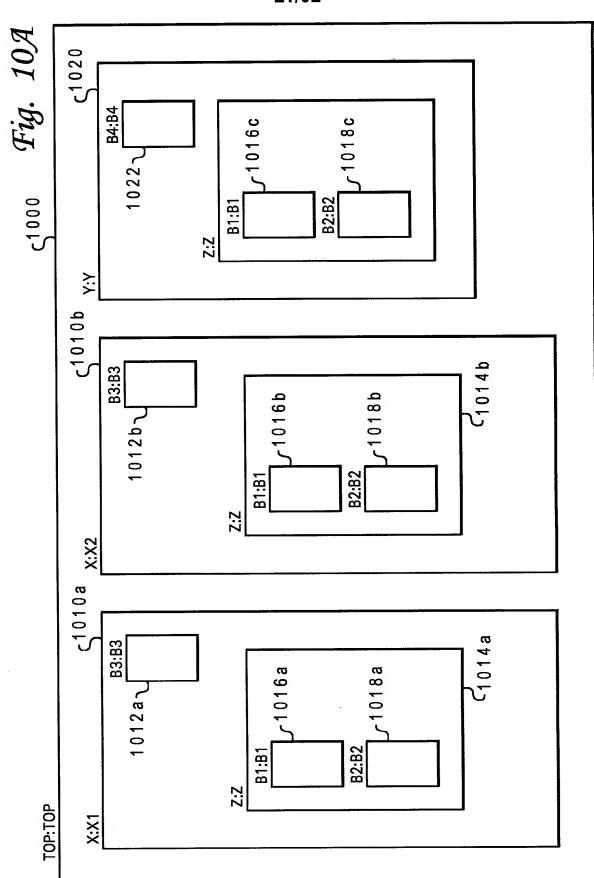
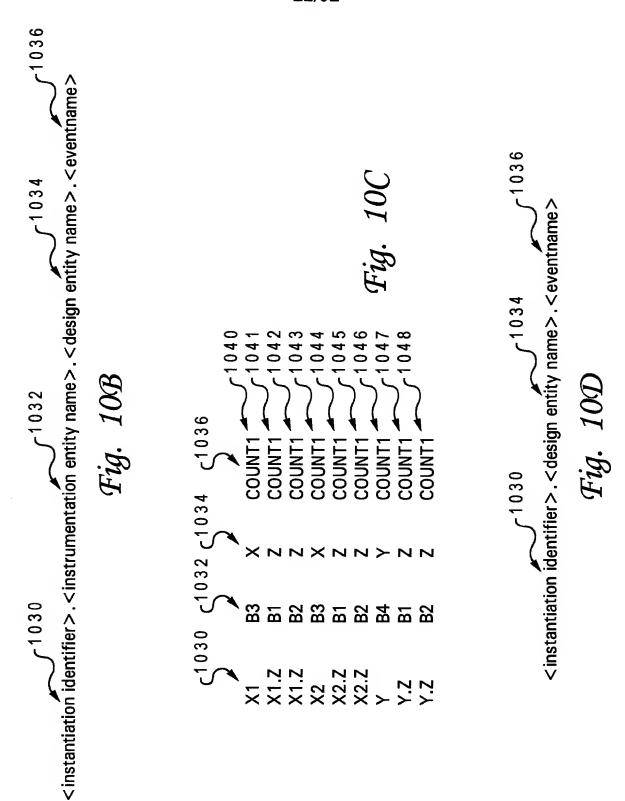
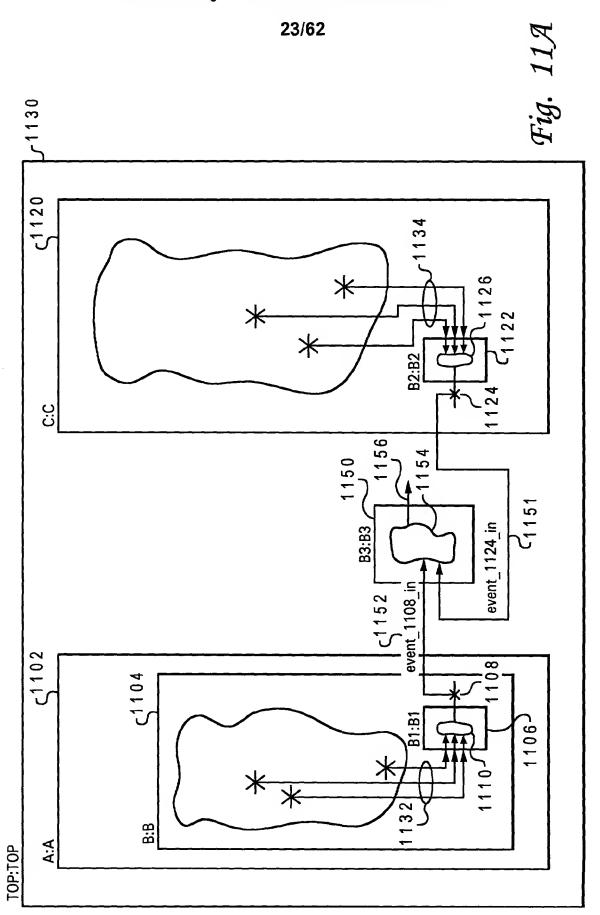


Fig. 9





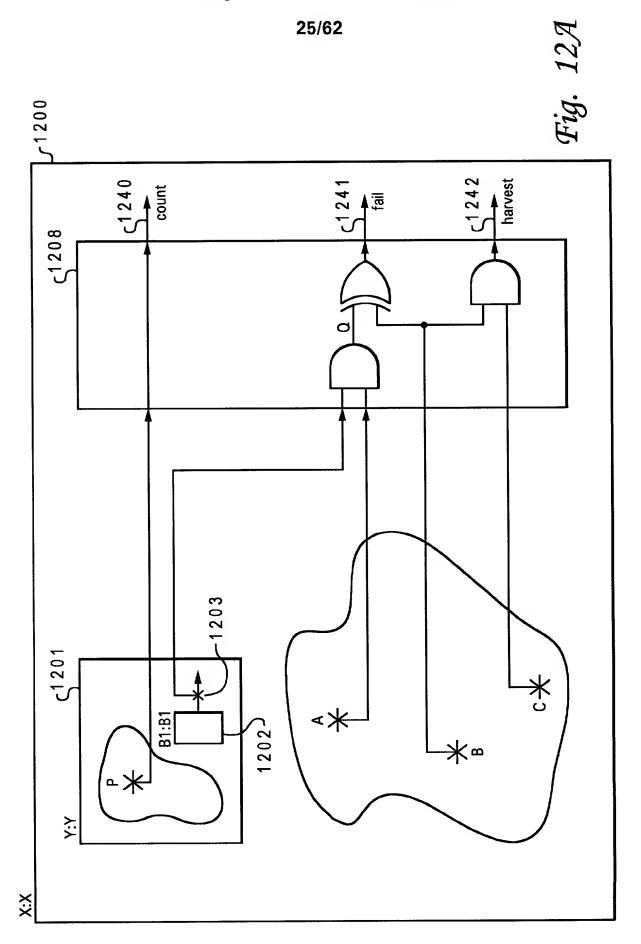


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```
--!! Inputs
--!! event_1108_in <= C.[B2.count.event_1108];
--!! event_1124_in <= A.B.[B1.count.event_1124];
--!! End Inputs
```

Fig. 11B

Fig. 11C



```
ENTITY X IS
       PORT(
          );
    ARCHITECTURE example of X IS
    BEGIN
      ... HDL code for X ...
                                        1220
END;
```

Fig. 12B

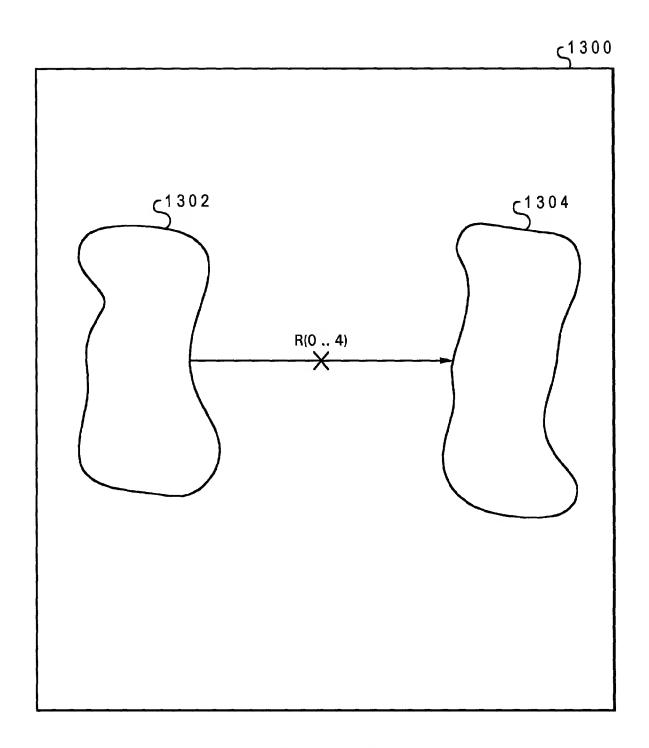
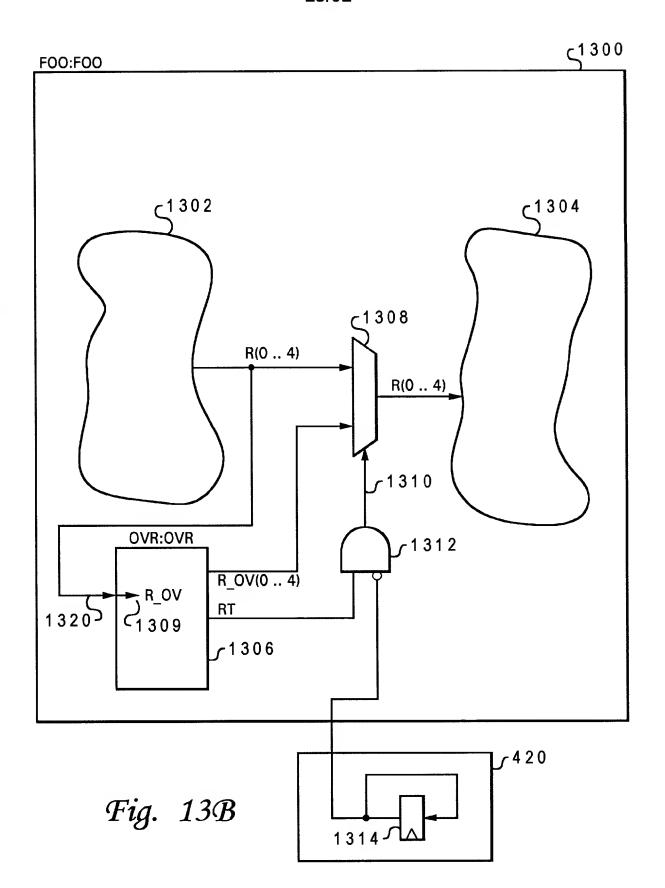


Fig. 13A



```
ENTITY OVR IS
      PORT(
                                  IN std_ulogic_vector(0 .. 4);
                ... other ports as required ...
                                                              1362
                             : OUT std_ulogic_vector(0 .. 4);
                                   OUT std ulogic
            );
--!! BEGIN
--!! Design Entity: FOO;
--!! Inputs (0 to 4)
--!! R IN = > \{R(0...4)\};
                                                                           1340
... other ports as needed ...
--!! :
                                                               1351
--!! End Inputs
--!! Outputs

--!! <R_OVRRIDE> : R_OV(0 .. 4) => R(0 .. 4) [RT];

--!! End Outputs
--!! End
ARCHITECTURE example of OVR IS
BEGIN
     ... HDL code for entity body section ...
END;
```

Fig. 13C

ENTITY FOO IS

```
PORT(
                                       );
               ARCHITECTURE example of FOO IS
               BEGIN

\begin{array}{c}
\vdots \\
\vdots \\
-!! R_IN <= \{R\}; \\
-!! C_1382 \\
-!! R_OV(0 \text{ to } 4) <= .....; \\
-!! RT <= .....; \\
-!! Ioverride, R_OVRRIDE, R(0 .. 4), RT] <= R_OV(0 \text{ to } 4);
\end{array}
```

Fig. 13D



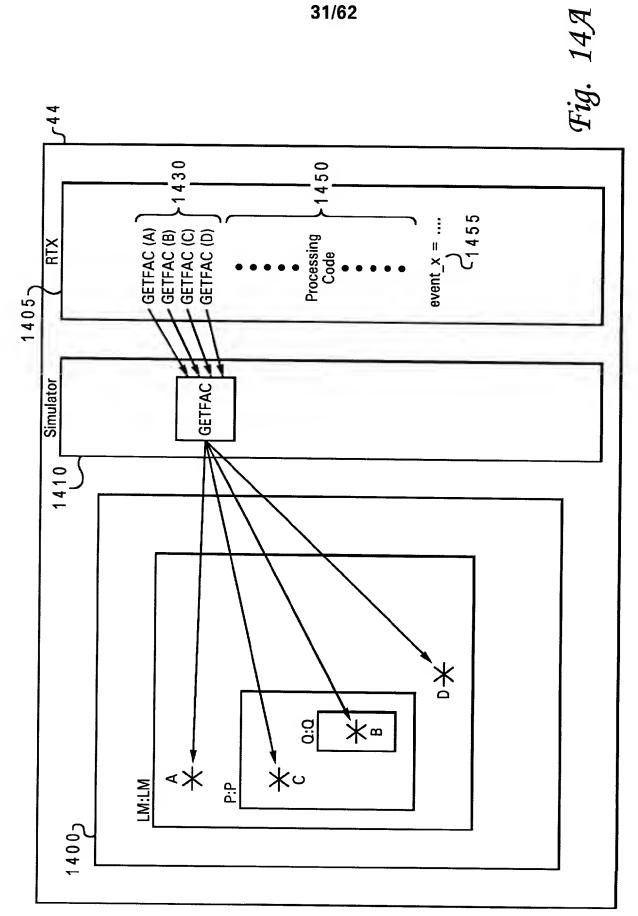
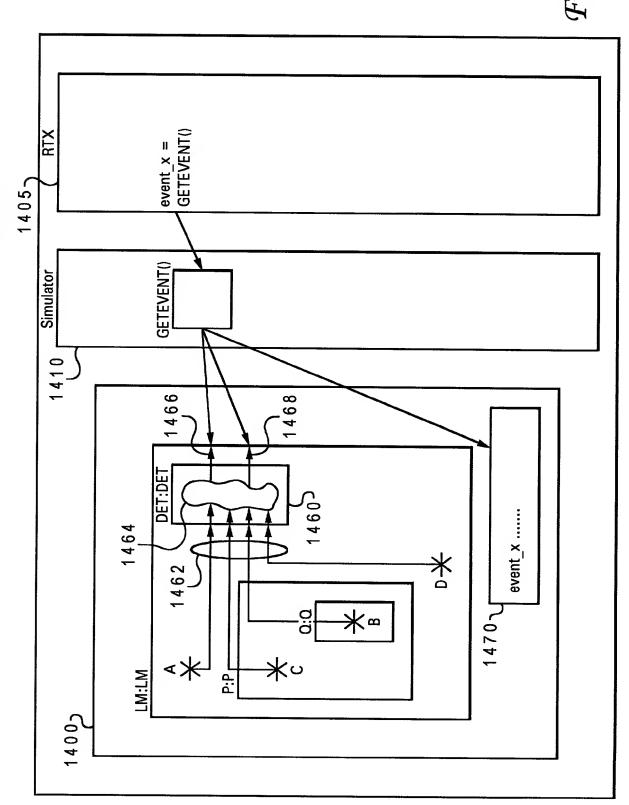


Fig. 14B



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```
ENTITY DET IS
      PORT(
                                      IN std ulogic;
                 В
                                      IN std_ulogic_vector(0 to 5);
                  C
                                      IN std ulogic;
                 D
                                      IN std ulogic;
                 event x
                                      OUT std ulogic vector(0 to 2);
                 x here
                                      OUT std ulogic;
             );
--!! BEGIN
-!! Design Entity: LM;
--!! Inputs
--!! B =>
--!! C =>
--!! D =>
--!! End Inputs
                  P.Q.B;
P.C;
                                                                             1480
--!! Detections
--!! <event_x>:event_x(0 to 2) [x_here];
--!! End Detections
--!! End;
ARCHITECTURE example of DET IS
BEGIN
      ... HDL code ...
END;
```

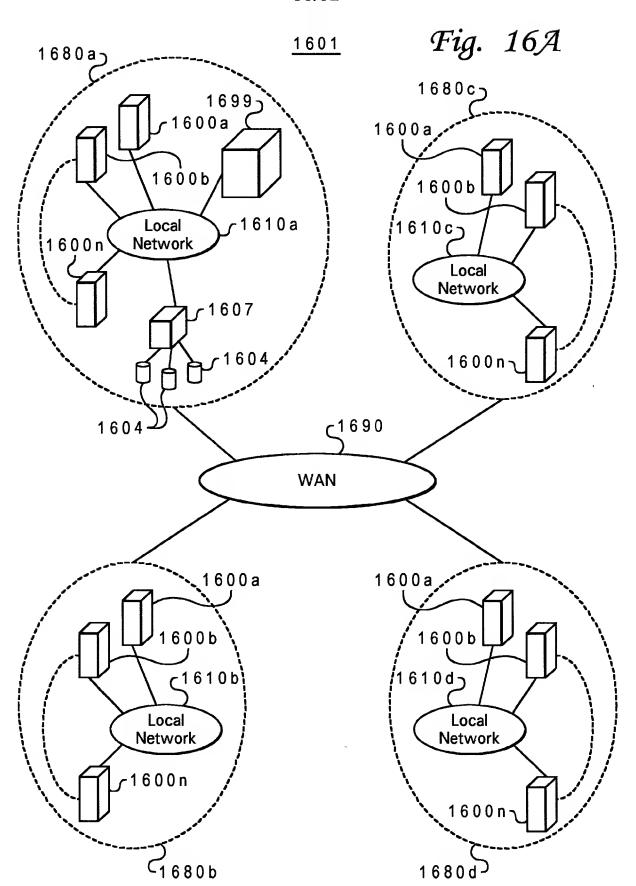
Fig. 14C

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| | | | | | 51660 |
|------|----|------|----|------|--------|
| 1661 | | | | 1662 | |
| ſ | 1: | X1 | В3 | X | COUNT1 |
| | 2: | X1.Z | B1 | Z | COUNT1 |
| | 3: | X1.Z | B2 | Z | COUNT1 |
| | 4: | X2 | В3 | X | COUNT1 |
| 1663 | 5: | X2.Z | B1 | Z | COUNT1 |
| | 6: | X2.Z | B2 | Z | COUNT1 |
| | 7: | Υ | B4 | Υ | COUNT1 |
| | 8: | Y.Z | B1 | Z | COUNT1 |
| | 9: | Y.Z | B2 | Z | COUNT1 |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

Fig. 15





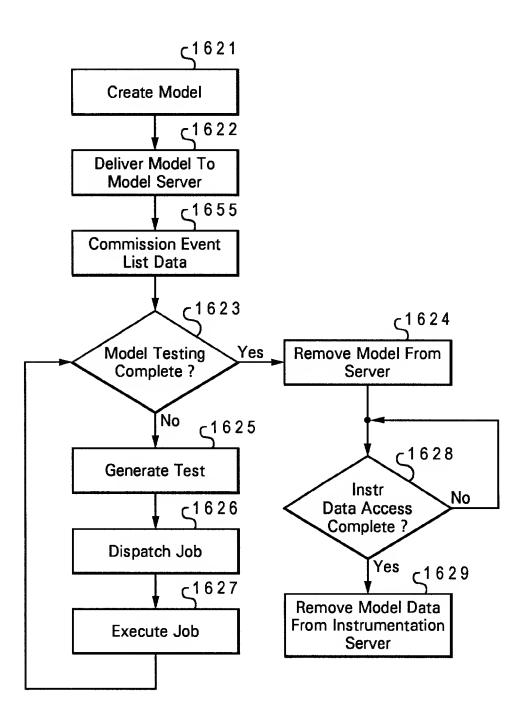
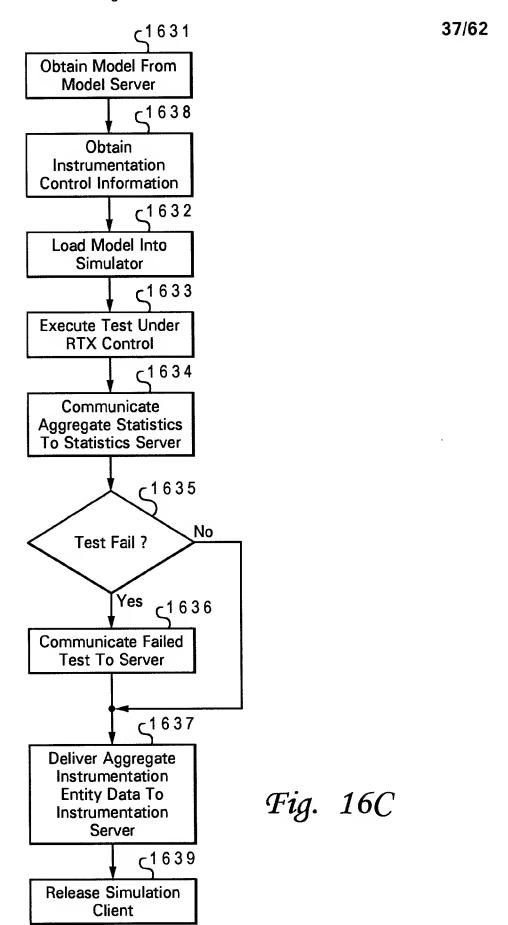


Fig. 16B



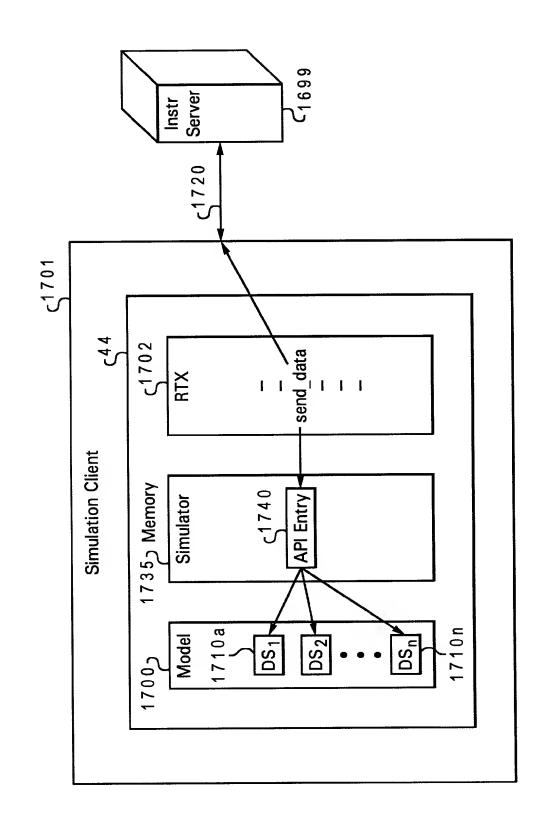


Fig. 17A

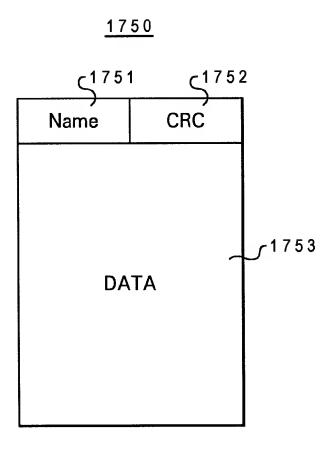


Fig. 17B

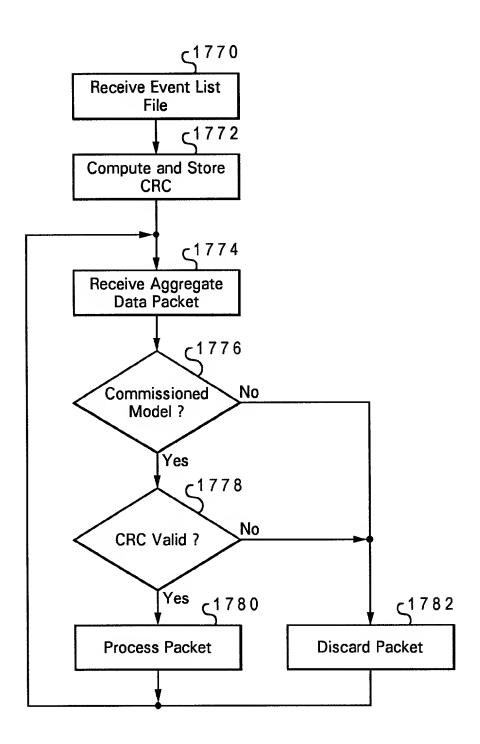


Fig. 17C

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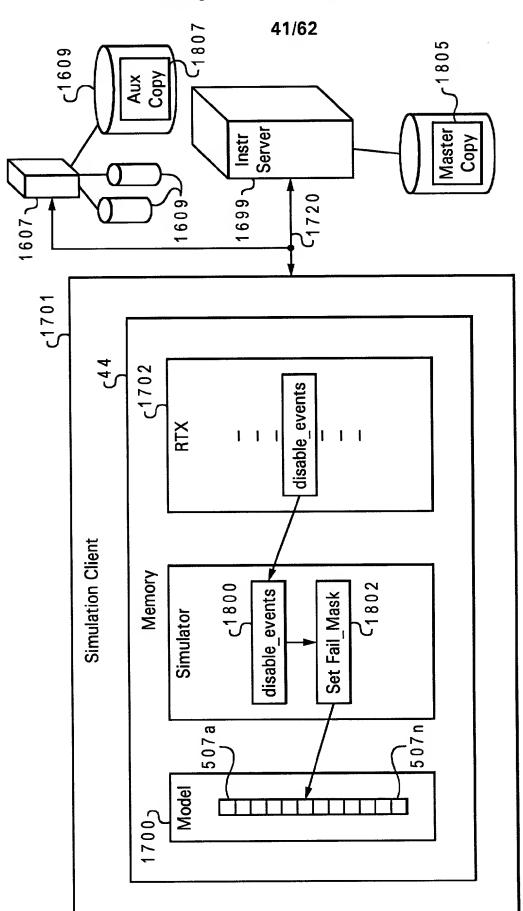
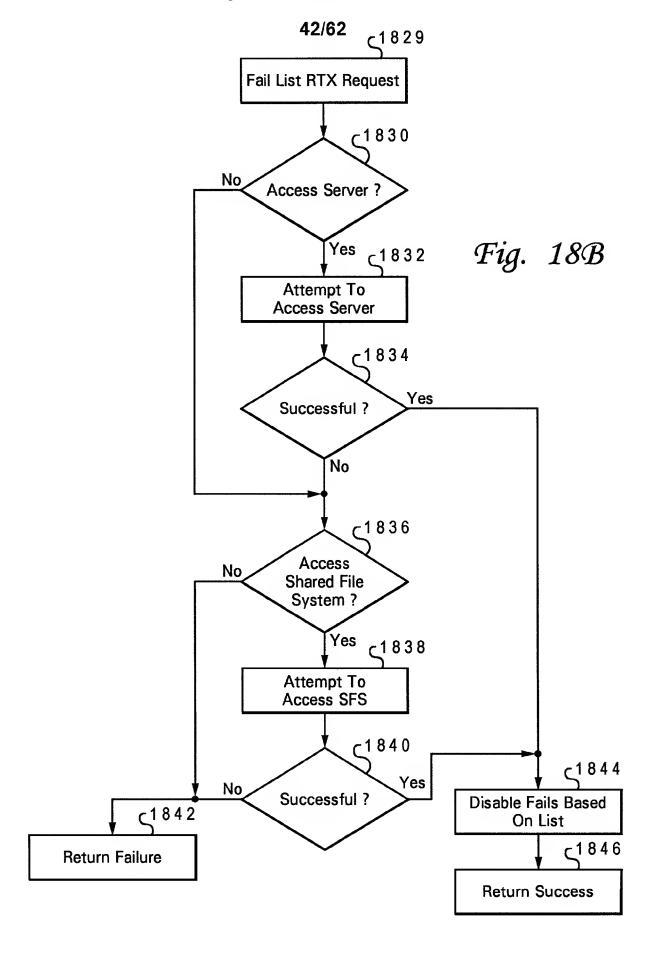


Fig. 18A

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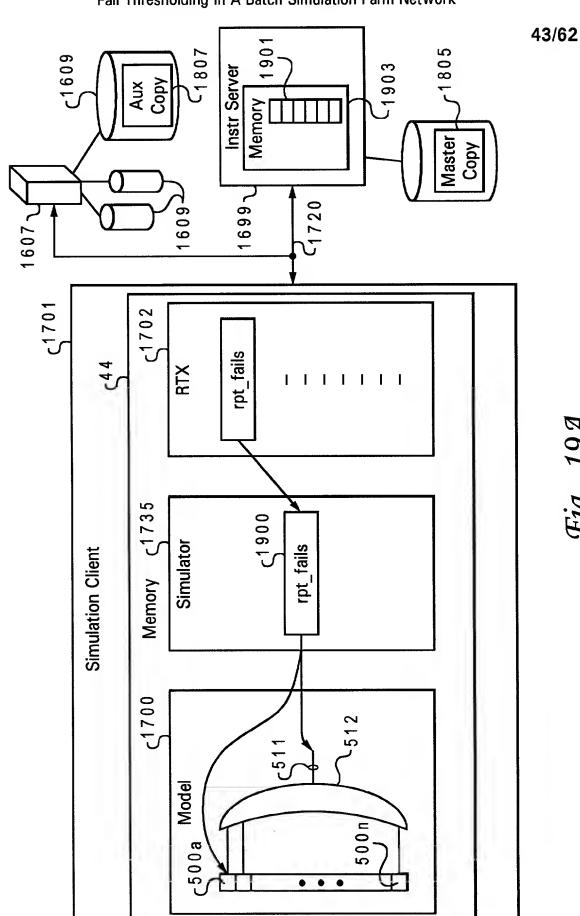
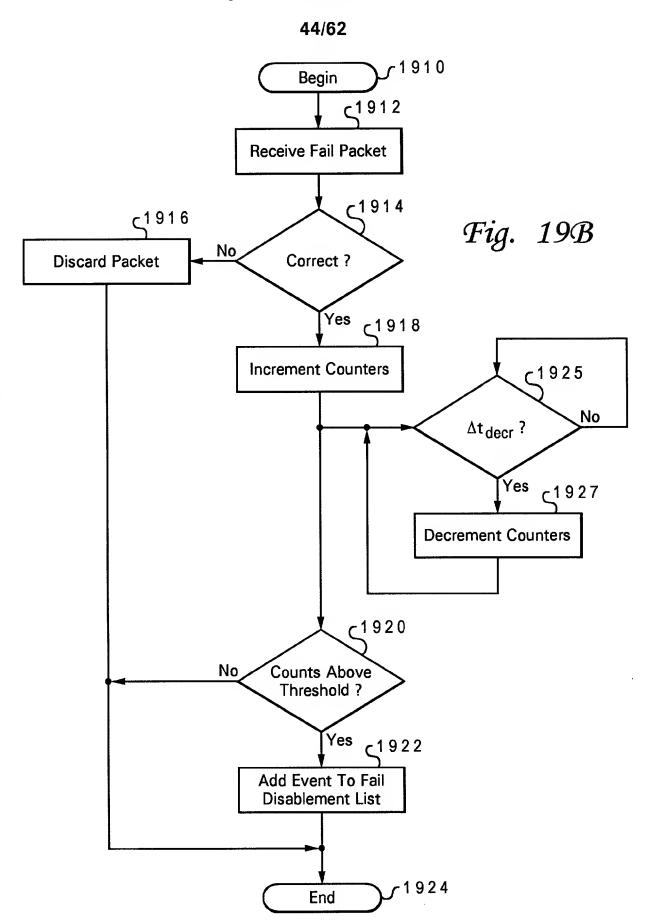


Fig. 19A



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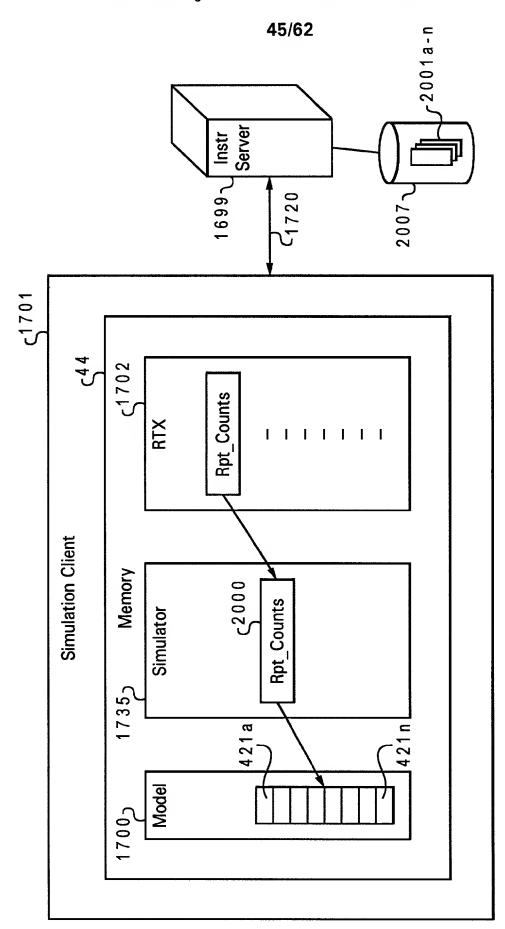


Fig. 20A

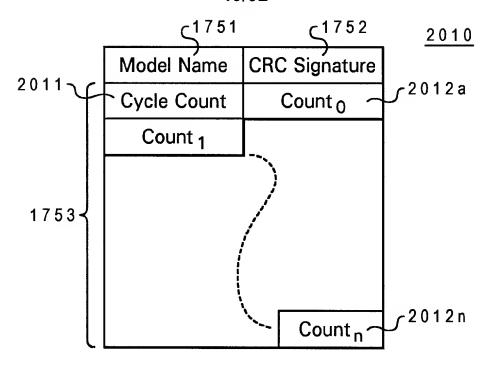


Fig. 20B

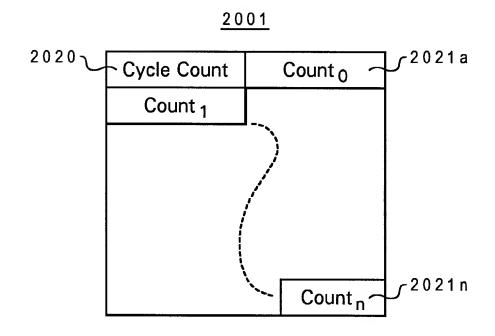


Fig. 20C

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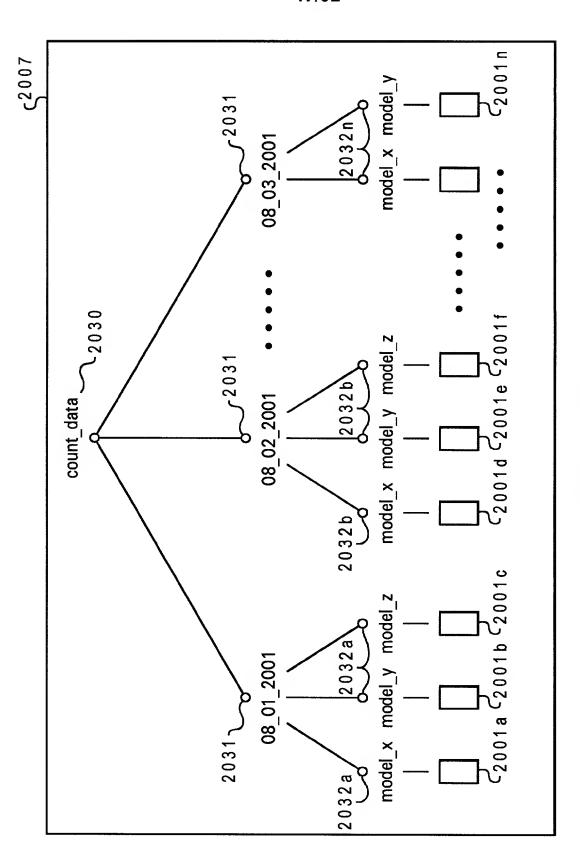


Fig. 20D

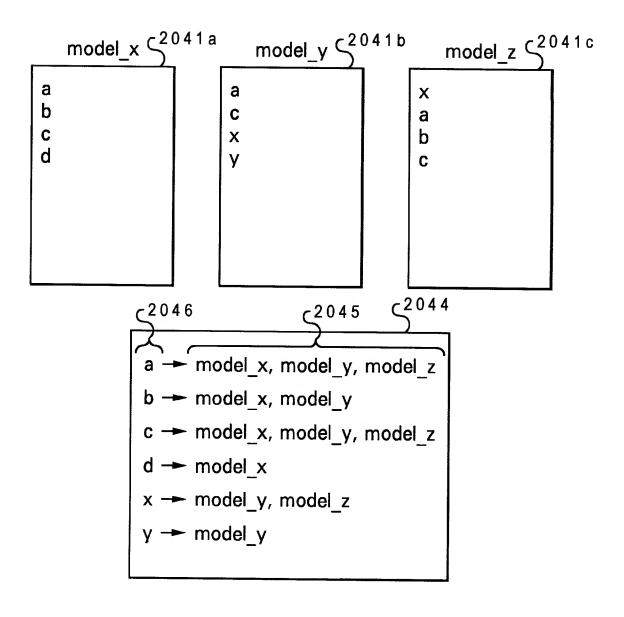
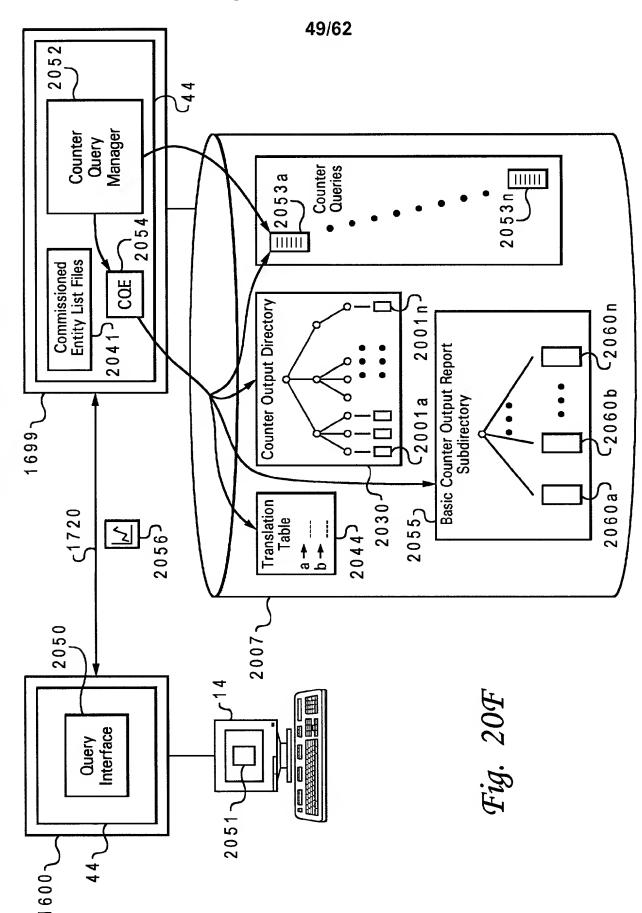
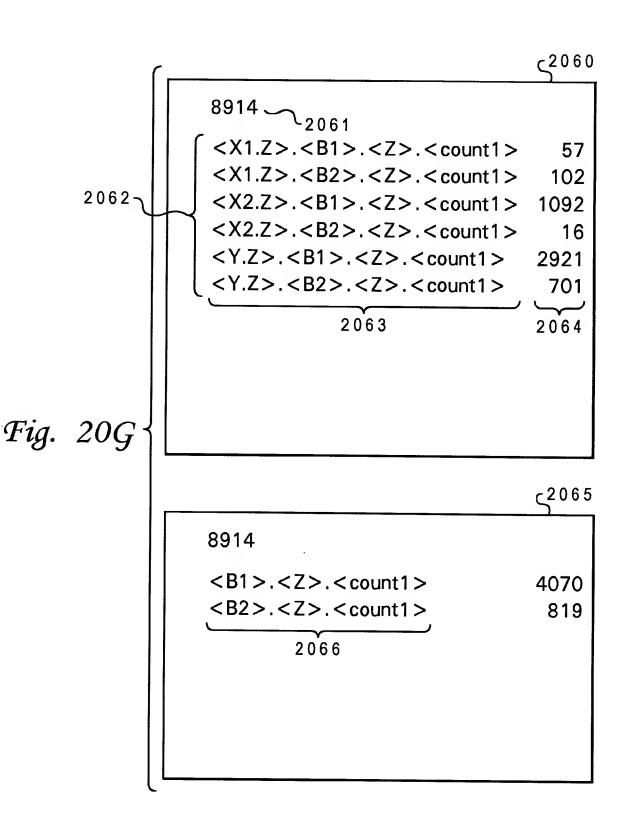


Fig. 20E

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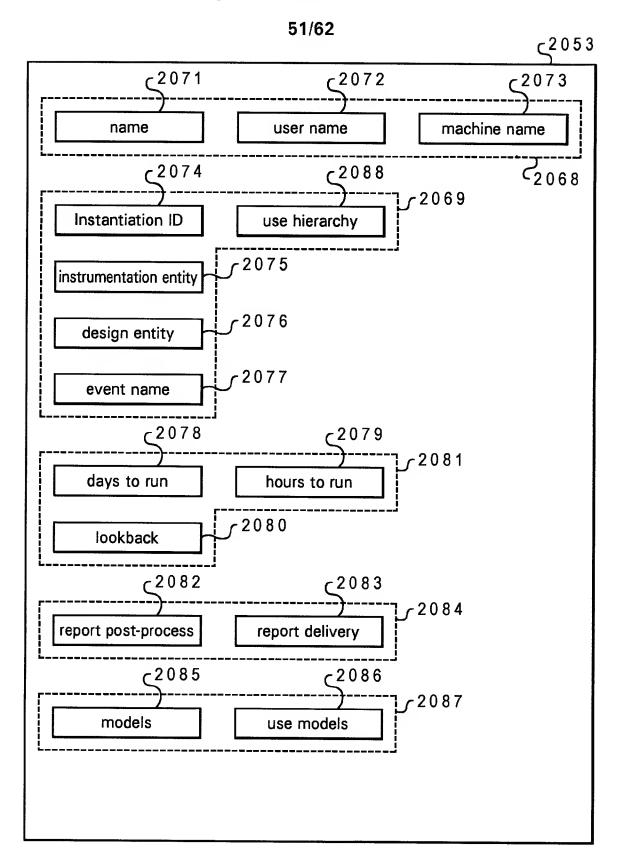


Fig. 20H

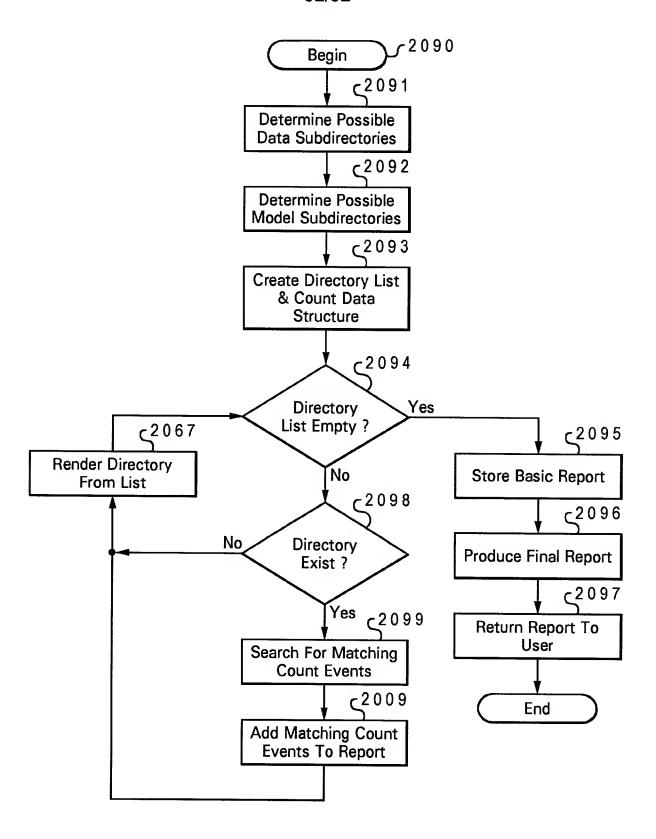
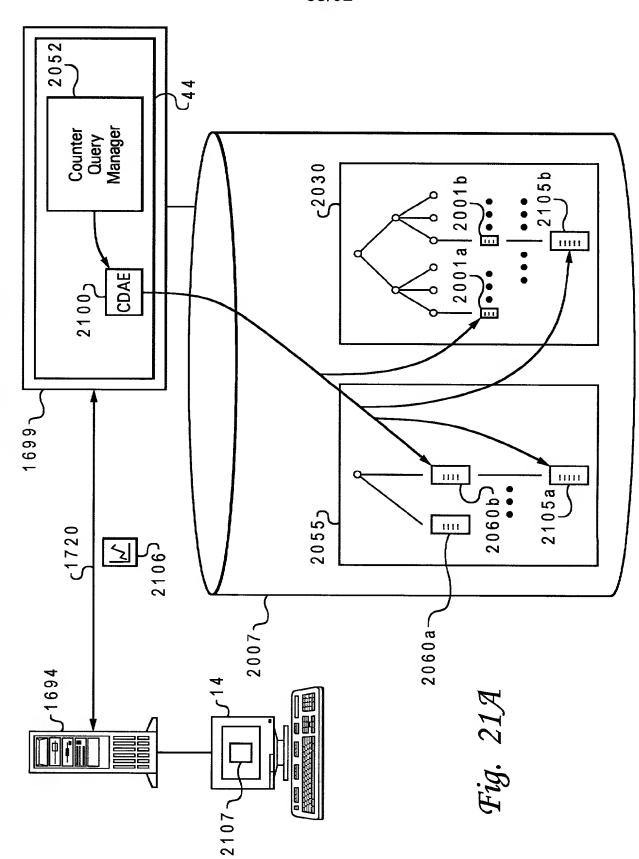


Fig. 201

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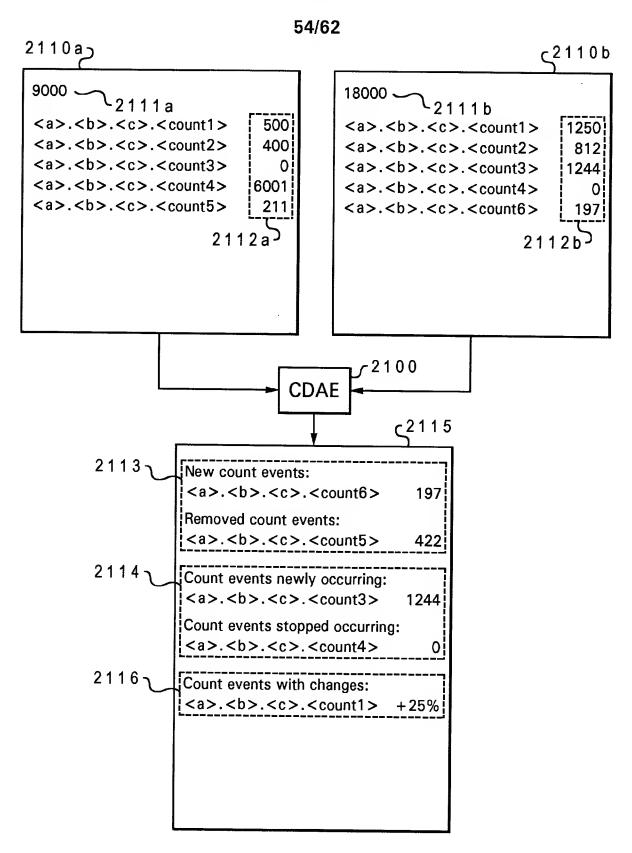


Fig. 21B

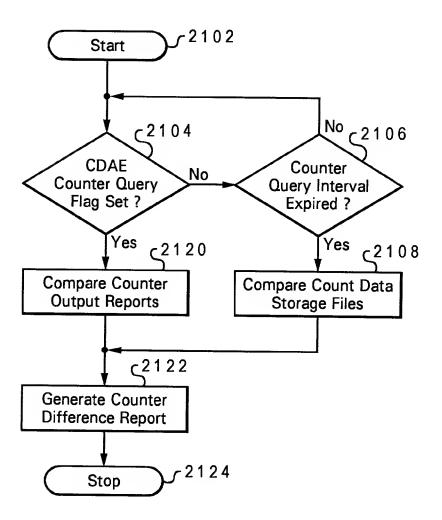
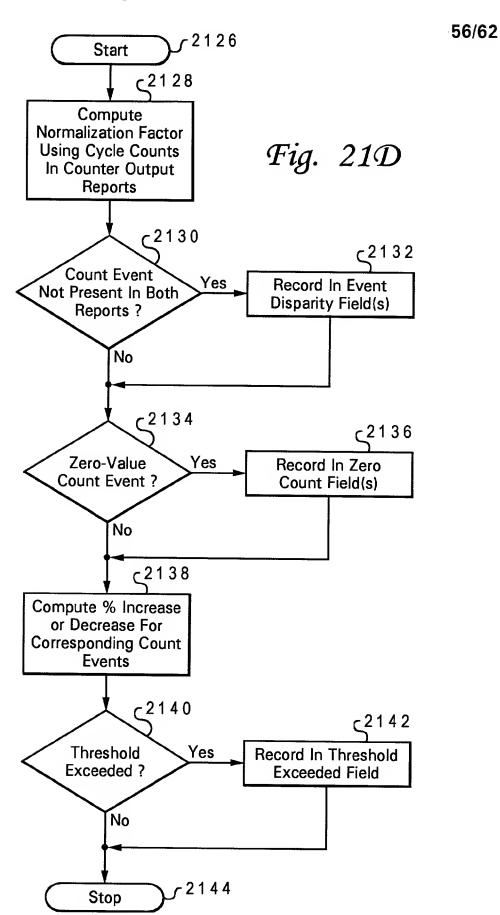
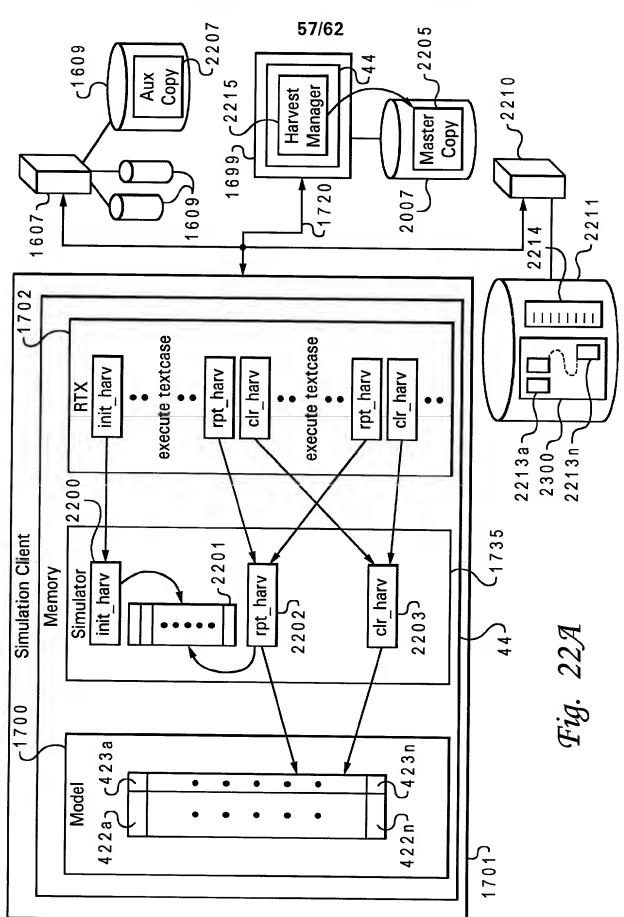
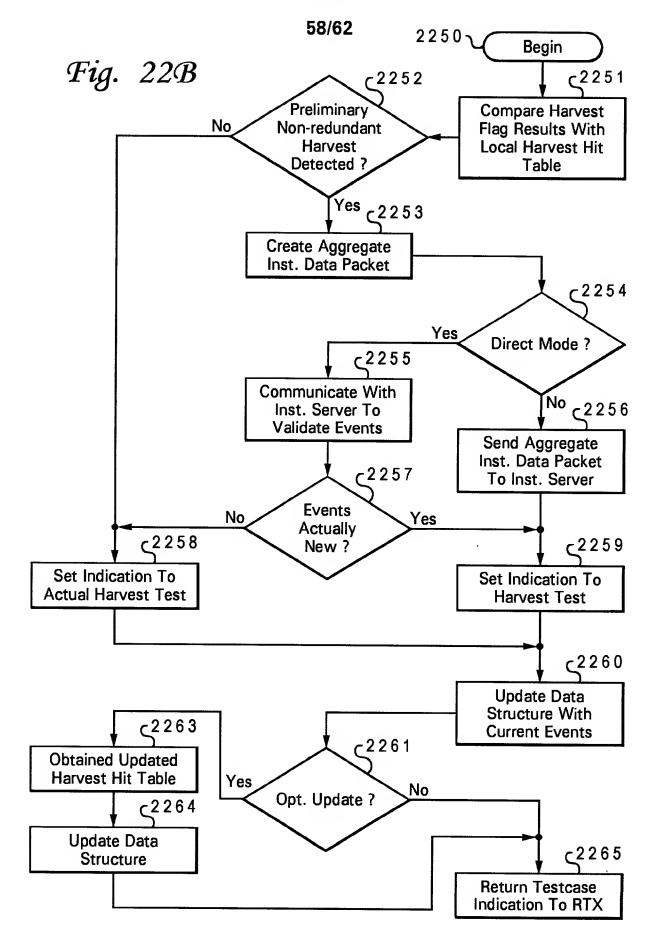


Fig. 21C

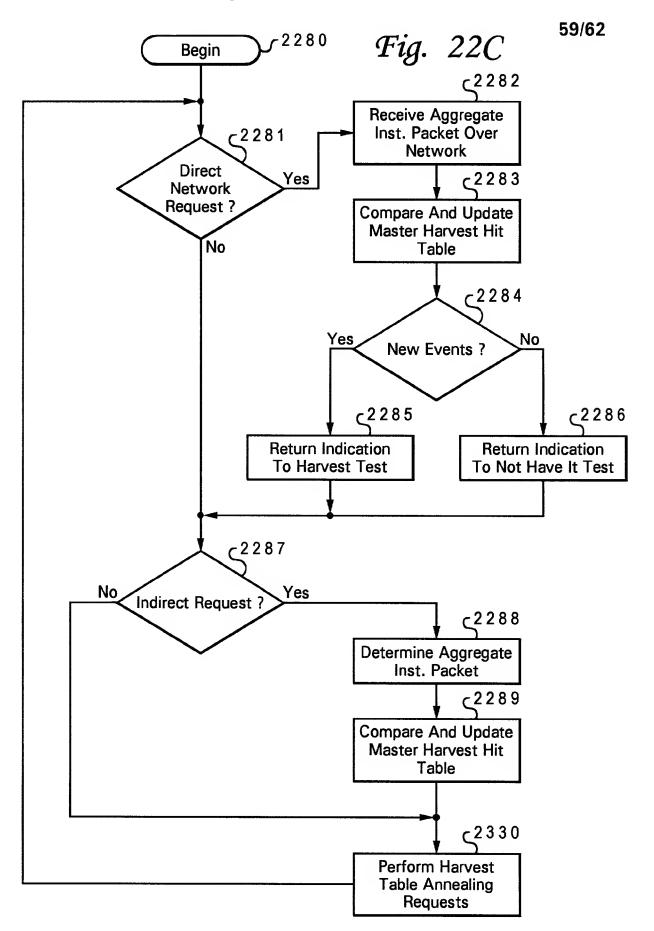


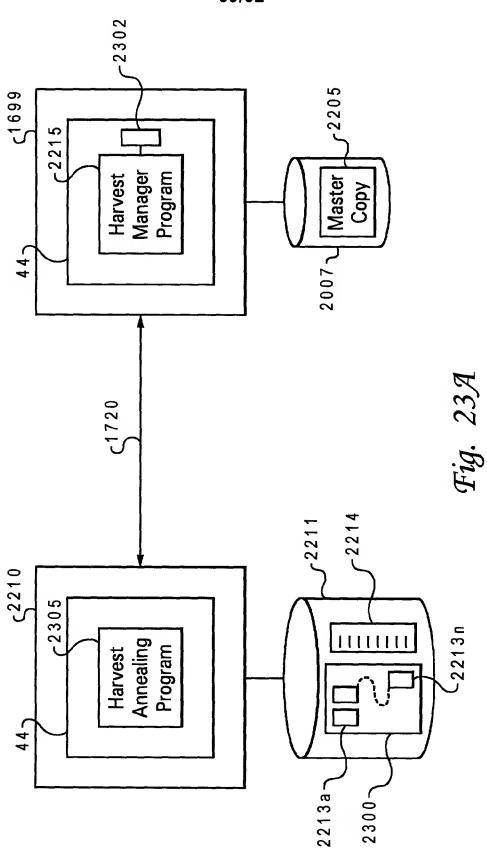
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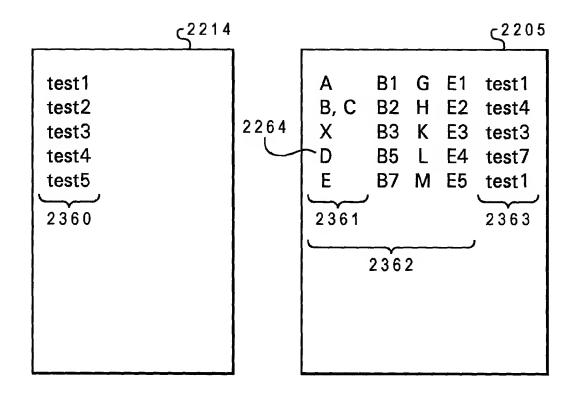


Fig. 23B

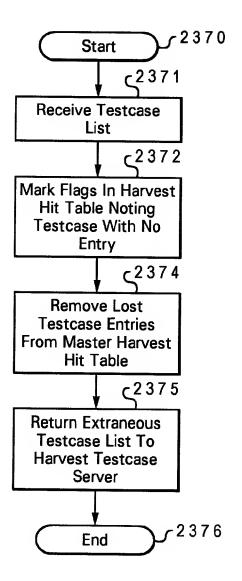


Fig. 23C